

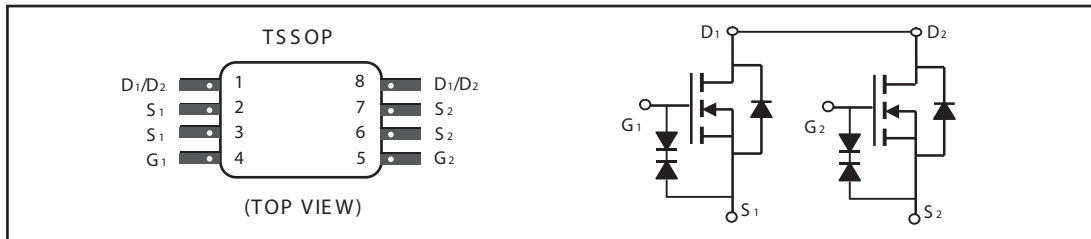


Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V _{DSS}	I _D	R _{DS(ON)} (mΩ) Max
20V	10A	13.5 @ V _{GS} = 4.0V
		18 @ V _{GS} = 2.5V

FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- Surface Mount Package.
- ESD Protected.



ABSOLUTE MAXIMUM RATINGS (T_A=25° C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	±12	V
Drain Current-Continuous ^a @ T _J =25° C -Pulsed ^b	I _D	10	A
	I _{DM}	40	A
Drain-Source Diode Forward Current ^a	I _S	1.7	A
Maximum Power Dissipation ^a	P _D	1.5	W
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ^a	R _{θJA}	85	°C/W
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ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16V, V_{GS} = 0V$			1	μA
Gate-Body Leakage	I_{GSS}	$V_{GS} = \pm 12V, V_{DS} = 0V$			± 10	μA
ON CHARACTERISTICS ^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.5	0.8	1.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 4V, I_D = 5A$		11	13.5	m ohm
		$V_{GS} = 2.5V, I_D = 3A$		13.5	18	m ohm
Forward Transconductance	g_{FS}	$V_{DS} = 5V, I_D = 5A$		22		S
DYNAMIC CHARACTERISTICS ^c						
Input Capacitance	C_{ISS}	$V_{DS} = 8V, V_{GS} = 0V$ $f = 1.0MHz$		1815		pF
Output Capacitance	C_{OSS}			406		pF
Reverse Transfer Capacitance	C_{RSS}			255		pF
SWITCHING CHARACTERISTICS ^c						
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = 10V,$ $I_D = 1A,$ $V_{GEN} = 4V,$ $R_L = 10\text{ ohm}$ $R_{GEN} = 10\text{ ohm}$		31		ns
Rise Time	t_r			62		ns
Turn-Off Delay Time	$t_{D(OFF)}$			96		ns
Fall Time	t_f			40		ns
Total Gate Charge	Q_g	$V_{DS} = 10V, I_D = 5A,$ $V_{GS} = 4V$		19		nC
Gate-Source Charge	Q_{gs}			3.5		nC
Gate-Drain Charge	Q_{gd}			6.7		nC

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ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS^b						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_s = 1.7A$		0.75	1.2	V

Notes

- a. Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.
- b. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.
- c. Guaranteed by design, not subject to production testing.

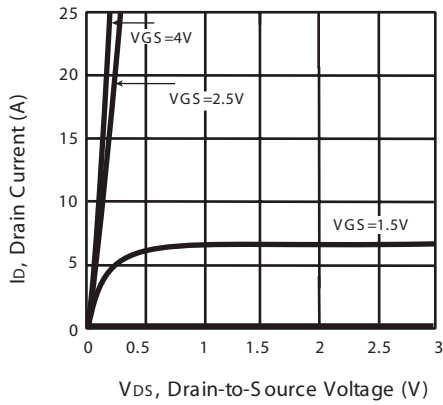


Figure 1. Output Characteristics

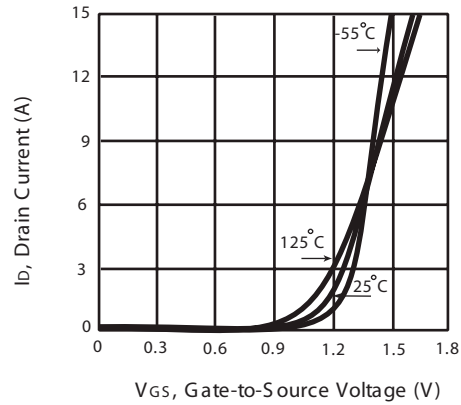


Figure 2. Transfer Characteristics

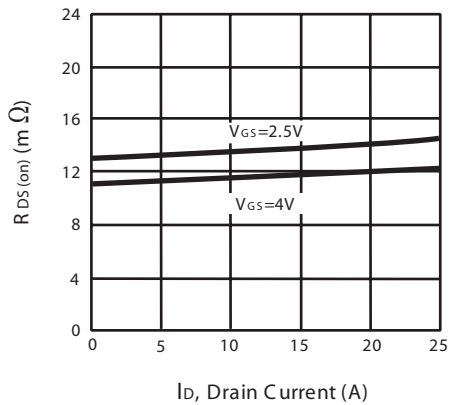


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

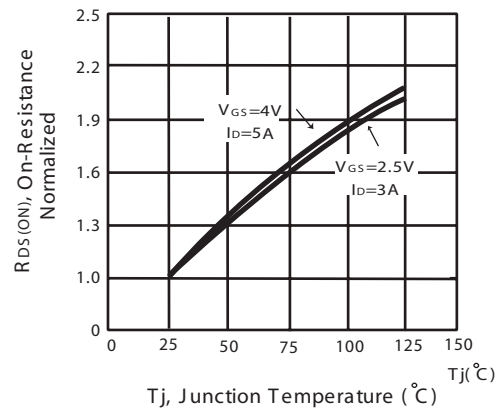


Figure 4. On-Resistance Variation with Drain Current and Temperature

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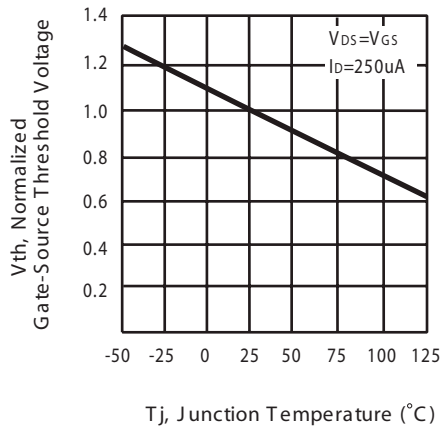


Figure 5. Gate Threshold Variation with Temperature

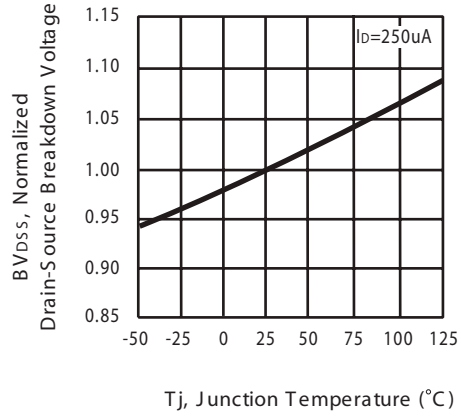


Figure 6. Breakdown Voltage Variation with Temperature

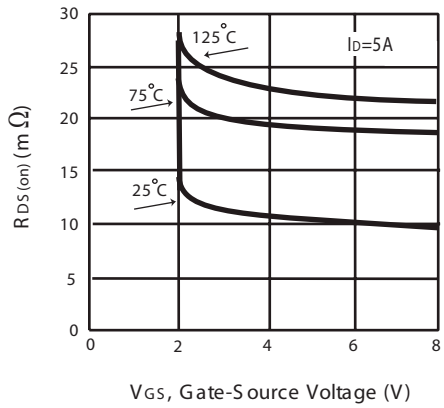


Figure 7. On-Resistance vs. Gate-Source Voltage

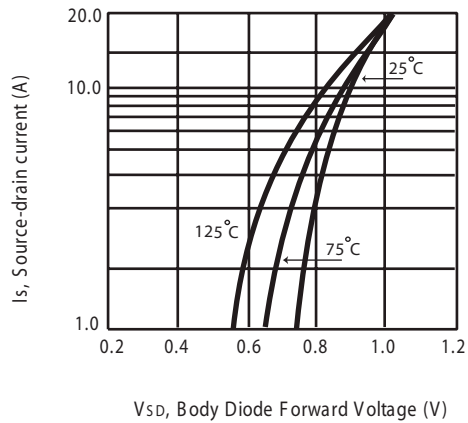
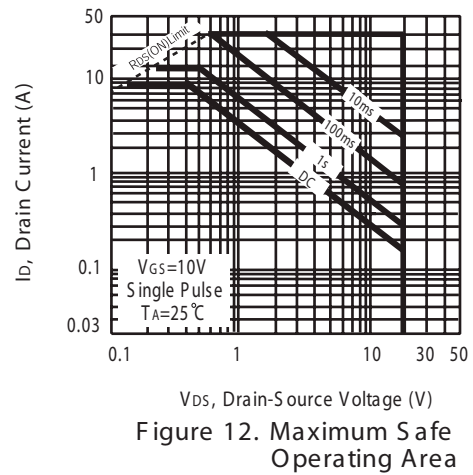
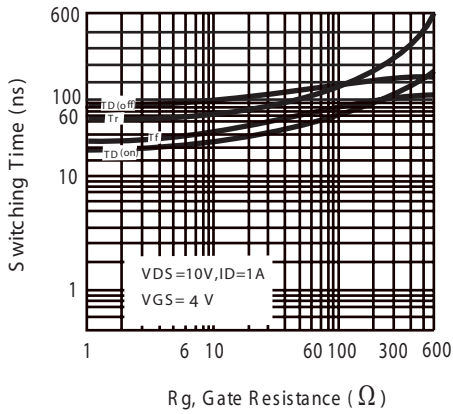
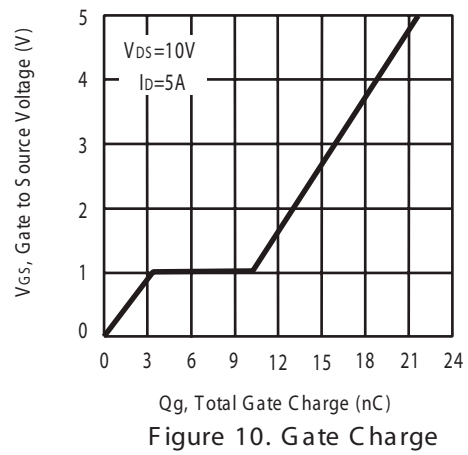
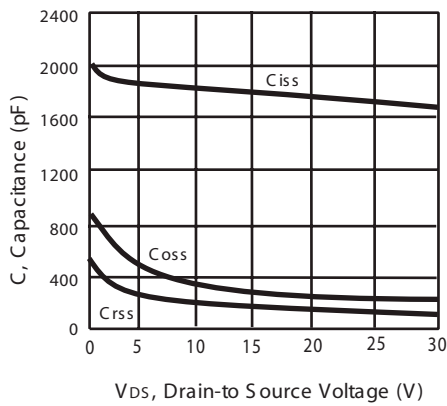


Figure 8. Body Diode Forward Voltage Variation with Source Current

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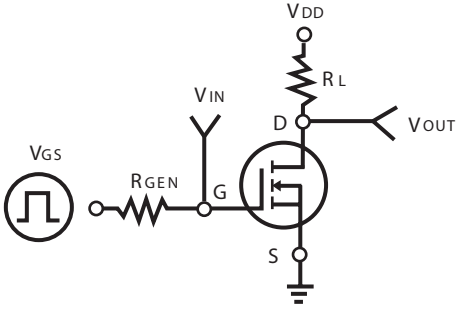


Figure 13. S switching Test Circuit

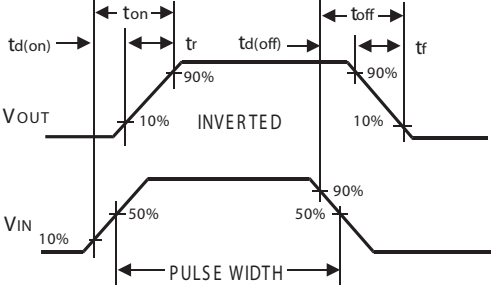


Figure 14. S switching Waveforms

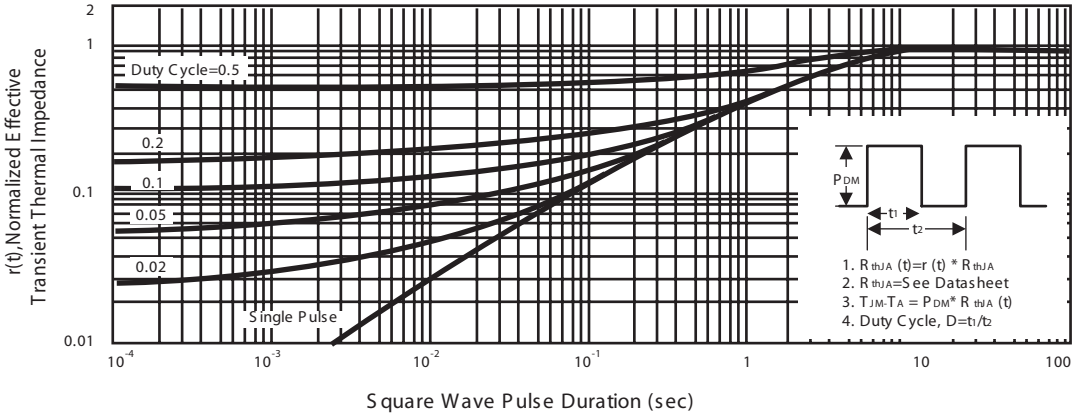
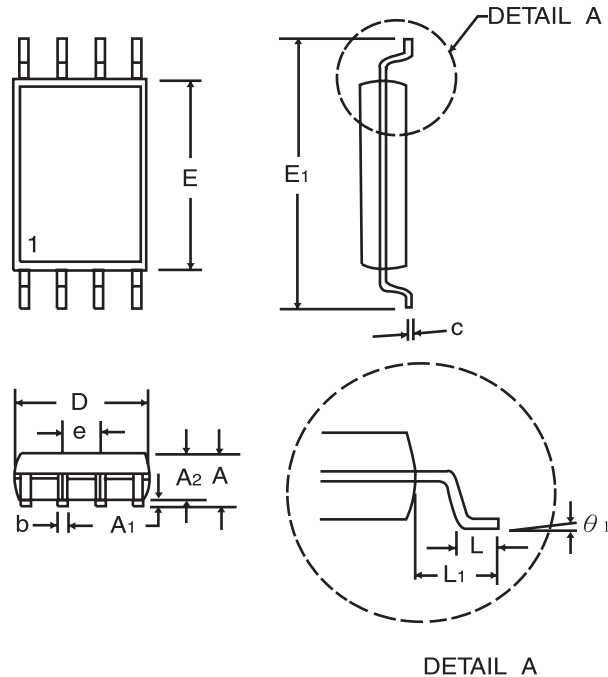


Figure 15. Normalized Thermal Transient Impedance Curve

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PACKAGE OUTLINE DIMENSIONS

TSSOP-8



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.85	1.20	0.033	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.127		0.005	
D	2.90	3.10 ^②	0.114	0.122 ^②
E	4.30	4.50 ^③	0.169	0.177 ^③
E1	6.20	6.60	0.244	0.260
e	0.65BSC		0.025BSC	
L	0.50	0.70	0.020	0.028
L1	1.00		0.039	
θ_1	0°	8°	0°	8°

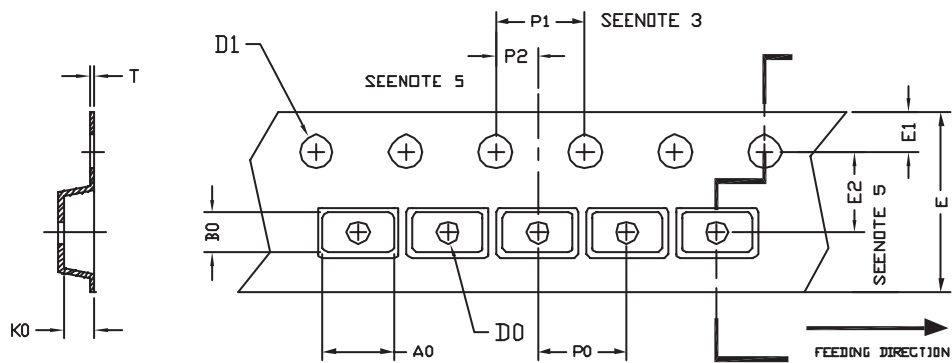
Notes:

1. This drawing is for general information only.
Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs.
Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E does not include inter-lead Flash or protrusions.
Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E to be determined at Datum Plane H.

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TSSOP-8 Tape and Reel Data

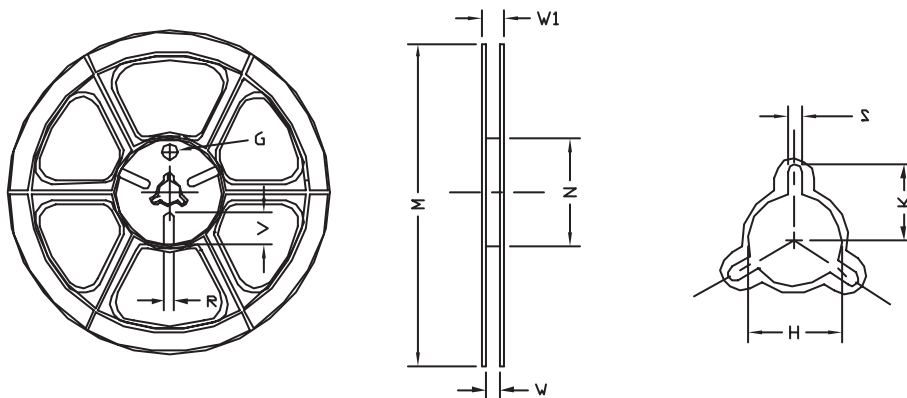
TSSOP-8 Carrier Tape



UNIT : mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TSSOP 8	6.08	4.40	1.60	ϕ 1.50 + 0.1 - 0.0	ϕ 1.50 + 0.1 - 0.0	12.00 \pm 0.3	1.75	5.50 \pm 0.05	8.00	4.00	2.00 \pm 0.05	0.30 \pm 0.05

TSSOP-8 Reel



UNIT : mm

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ϕ 330	330	100	12.5	16.0	ϕ 13.0 + 0.5 - 0.2	10.6	2.0 \pm 0.5	---	---	---